4Mbit Asynchronous Low Power Static RAM

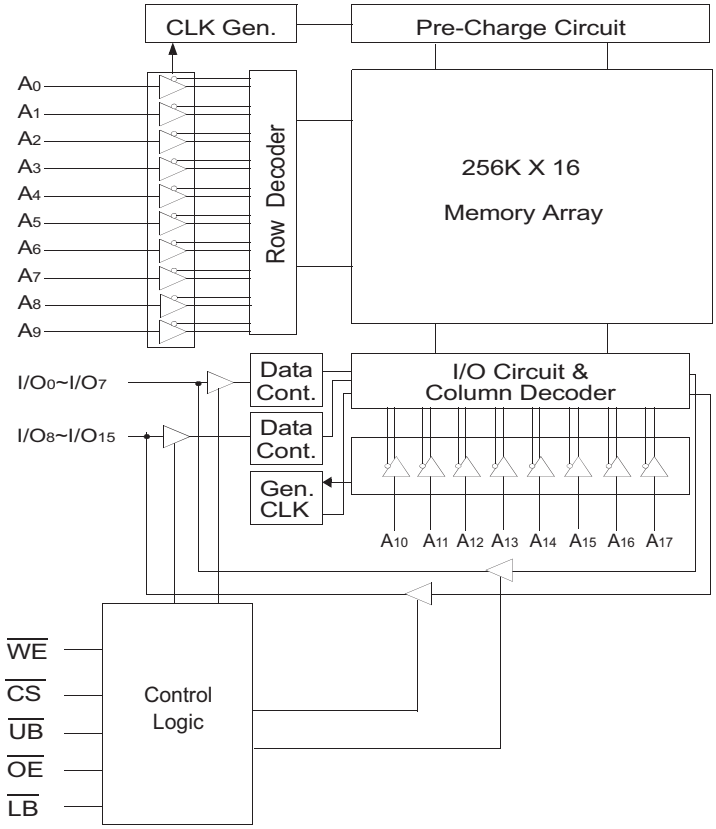
Features

- Process Technology : 90nm Full CMOS
- Organization : 256K x 16 bit
- Power Supply Voltage : 2.7V ~ 3.6V
- Low Data Retention Voltage : 1.5V(Min.)
- Three state output and TTL Compatible
- Standard 44TSOP2,48FBGA
- Industrial Operation Temperature.

Description

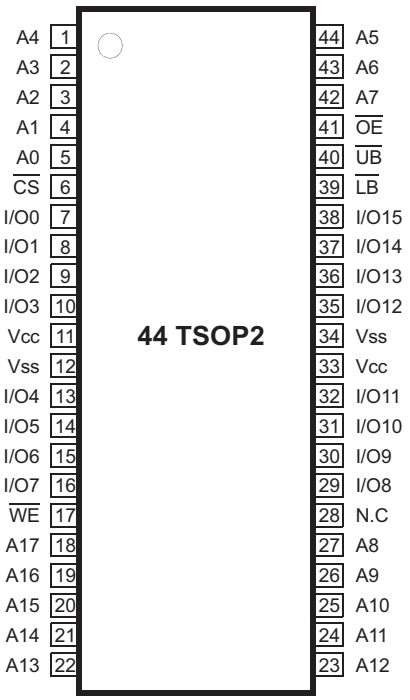
The device families are fabricated by EMI's advanced full CMOS process technology. The families support industrial temperature range and Chip Scale Package for user flexibility of system design. The families also supports low data retention voltage for battery back- up operation with low data retention current.

Logic Block Diagram

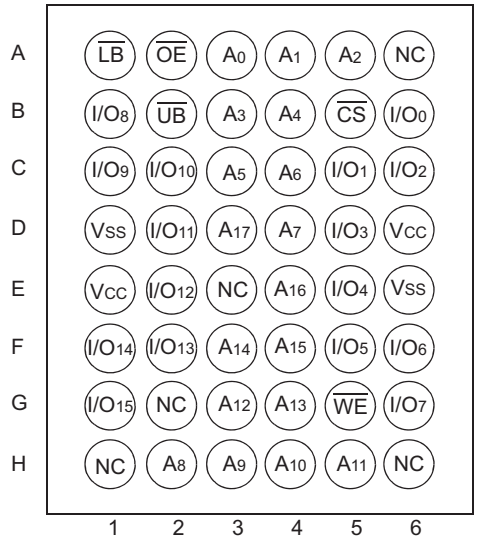


Package Pin Configurations

44TSOP2



48FBGA



Pin Description

Pin Name	Pin Function
A_0~A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control(I/O8~I/O15)
$\overline{LB}$	Lower Byte Control(I/O0~I/O7)
I/O_0 ~ I/O_{15}	Data Inputs/Outputs
N.C	No Connection
V_{CC}	Power
V_{SS}	Ground

Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Unit
P_D	Power Dissipation	1.0	W
Vcc	Voltage on Vcc supply relative to Vss	-0.5 to 4.6	V
T_A	Operating Temperature	-40 to 85	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to Vss	-0.5 to Vcc+0.5	V

Note:1, Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only andfunctional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Functional Description

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O_0~I/O_7	I/O_8~I/O_{15}	Power
H	X	X	X	X	Deselected	High-Z	High-Z	Stand by
X	X	X	H	H	Deselected	High-Z	High-Z	Stand by
L	H	H	L	X	Output Disable	High-Z	High-Z	Active
L	H	H	X	L	Output Disable	High-Z	High-Z	Active
L	H	L	L	H	Lower Byte Read	Data Out	High-Z	Active
L	L	X	L	H	Lower Byte Write	Data In	High-Z	Active
L	H	L	H	L	Upper Byte Read	High-Z	Data Out	Active
L	L	X	H	L	Upper Byte Write	High-Z	Data In	Active
L	H	L	L	L	Word Read	Data Out	Data Out	Active
L	L	X	L	L	Word Write	Data In	Data In	Active

Note : X means don't care. (Must be low or high state)

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	2.7	3.3	3.6	V
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.2	V
V_{IL}	Input Low Voltage	-0.2	-	0.6	V
V_{SS}	Ground	0	0	0	V

Capacitance*(TA=25°C, f=1.0MHz)

Symbol	Item	Test Conditions	Typ.	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	-	8	pF
C_{IN}	Input Capacitance	V_{IN}=0V	-	6	pF

DC and Operating Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	V_{IN}=V_{SS} to V_{CC}	-1	-	1	uA
I_{LO}	Output Leakage Current	$\overline{CS}$ =V_{IH} or $\overline{OE}$ =V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc	-1	-	1	uA
I_{CC}	Operating Current	f=fmax,V_{CC}= V_{CCmax}, I_{OUT}=0mA, V_{IN}≧ V_{CC} -0.2V or V_{IN}≦0.2V	-	-	20	mA
I_{CC1}		f=1MHz, VCC=V_{CCmax}, I_{OUT}=0mA, V_{IN} ≧ V_{CC} -0.2V or V_{IN}≦0.2V	-	-	3	mA
I_{SB}	Standby Current	V_{CC} = V_{CC} max, $\overline{CS}$=V_{IH}, Others=V_{IH} or V_{IL}	-	-	0.3	uA
I_{SB1}		V_{CC}=VCCmax, V_{IN}≧V_{CC} -0.2V or V_{IN}≦0.2V, $\overline{CS}$≧V_{CC} -0.2V, or $\overline{CS}$≦0.2V, $\overline{UB}$=$\overline{LB}$≧V_{CC} -0.2V	-	2	10	uA
V_{OL}	Output Low Voltage Level	I_{OL}=2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage Level	I_{OH}=-1.0mA	2.4	-	-	V

Test Conditions

Input Pulse Level : 0.4 to 2.2V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : 1.5V
Output Load (See right) : CL1) = 30pF + 1 TTL (55ns)

1. Including scope and Jig capacitance
2. R1=3070Ω, R2=3150Ω
3. VTM=2.8V
4. CL = 5pF + 1 TTL (measurement with t_{LZ}, t_{HZ}, t_{OLZ}, t_{OHZ}, t_{WHZ})

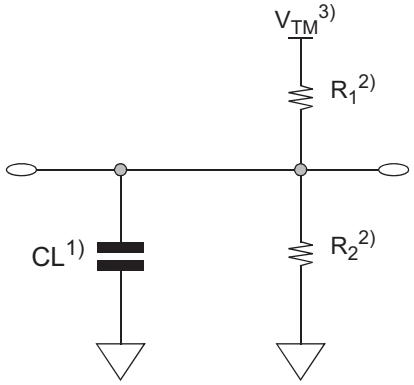


Figure1

Data Retention Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	Vcc for Data Retention	$\overline{CS} \geq V_{CC}$ -0.2V, Other inputs = 0~V_{CC}	1.5	-	3.6	V
I_{DR}	Data Retention Current	V_{CC}=1.5V $\overline{CS} \geq V_{CC}$ - 0.2V, Other inputs = 0~V_{CC}	-	2	10	uA
t_{SDR}	Data Retention Set-Up Time	See Figure 2(Data Retention Wave Form	0	-	-	ns
t_{RDR}	Recovery Time		t_{RC}	-	-	ns

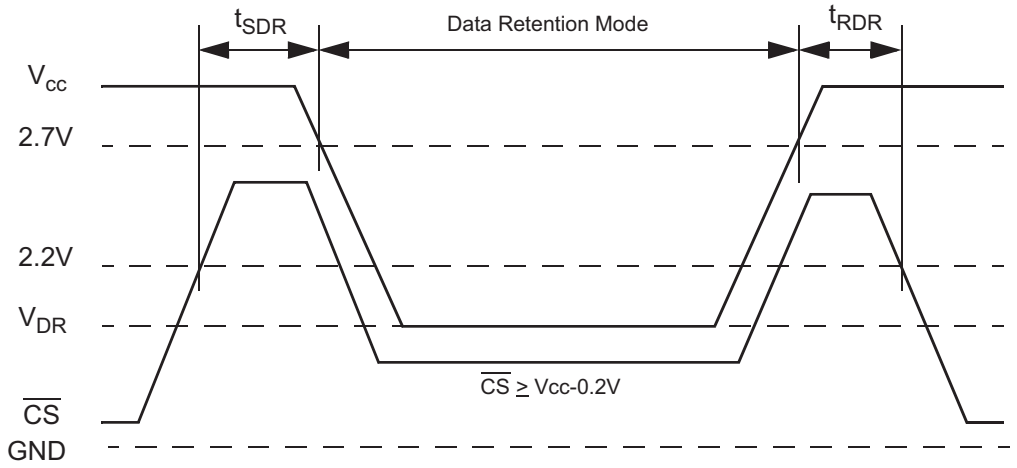


Figure 2 Data Retention Wave Form

Read Cycle

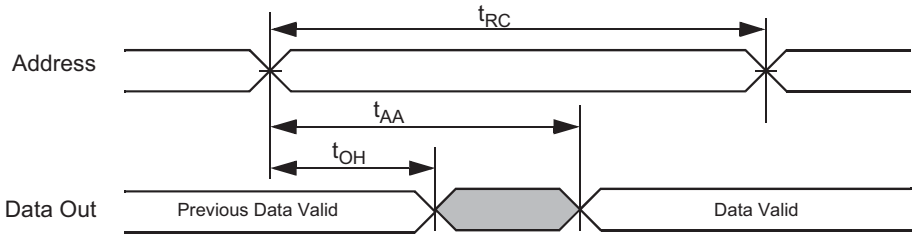
Symbol	Parameter	45ns		55ns		70ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	45	-	55	-	70	-	ns
t_{AA}	Address Access Time	-	45	-	55	-	70	ns
t_{OH}	Output Hold from Address Change	10	-	10	-	10	-	ns
t_{CO}	Chip Select to Output	-	45	-	55	-	70	ns
t_{OE}	Output Enable to Valid Output	-	22	-	25	-	35	ns
t_{LZ}	Chip Enable to Low-Z Output	10	-	10	-	10	-	ns
t_{OLZ}	Output Enable to Low-Z Output	5	-	5	-	5	-	ns
t_{HZ}	Chip Disable to High-Z Output	0	18	0	20	0	25	ns
t_{OHZ}	Output Disable to High-Z Output	0	18	0	20	0	25	ns
t_{BA}	UB, LB Access Time	-	45	-	55	-	70	
t_{BLZ}	UB, LB Low to Low-Z Output	5	-	5	-	5	-	
t_{BHZ}	UB, LB High to High-Z Output	-	18	0	20	0	25	

Write Cycle

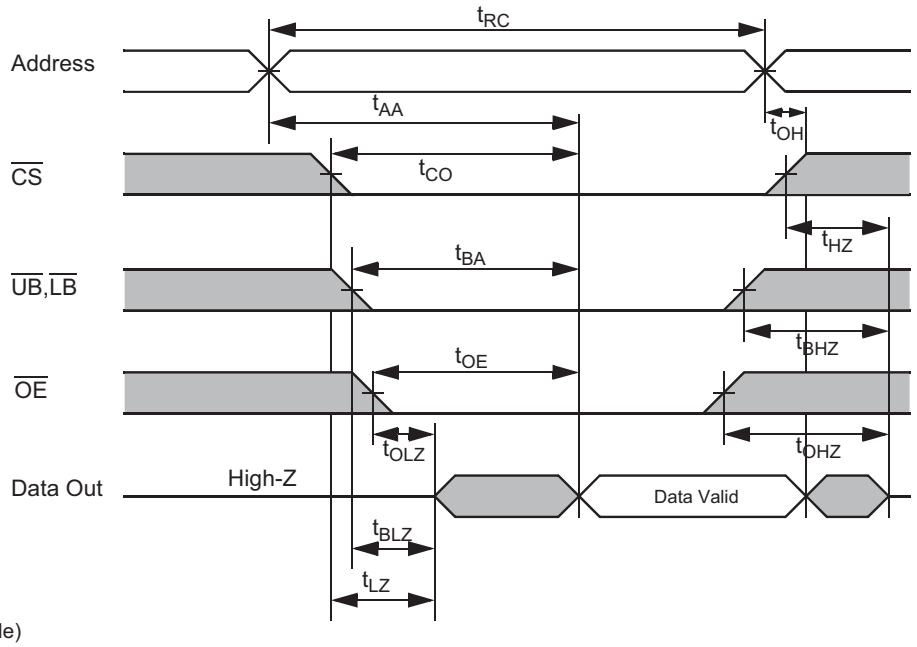
Symbol	Parameter	45ns		55ns		70ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	45	-	55	-	70	-	ns
t_{CW}	Chip Select to End of Write	35	-	45	-	60	-	ns
t_{AS}	Address Set-up Time	0	-	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	35	-	45	-	60	-	ns
t_{WP}	Write Pulse Width	35	-	40	-	55	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{WHZ}	Write to Output High-Z	0	18	0	20	0	20	ns
t_{DW}	Data to Write Time Overlap	25	-	25	-	30		ns
t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{OW}	End of Write to Output Low-Z	5	-	5	-	5	-	ns
t_{BW}	$\overline{UB}$, $\overline{LB}$ Low to End of Write	35	-	45	-	60	-	ns

Timing Diagrams

Timing Waveform Of Read Cycle(1)(Address Controlled)



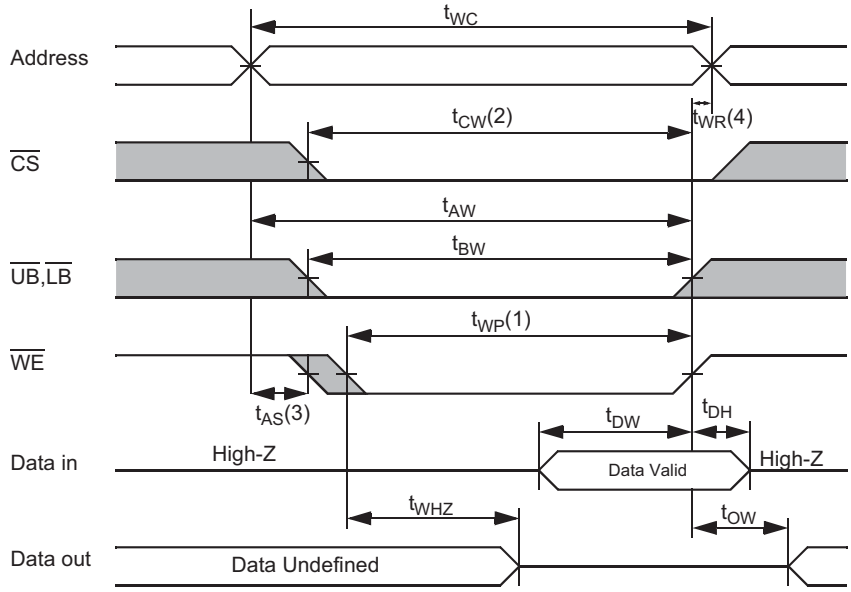
Timing Waveform Of Read Cycle(2)($\overline{WE}$=V_{IH})



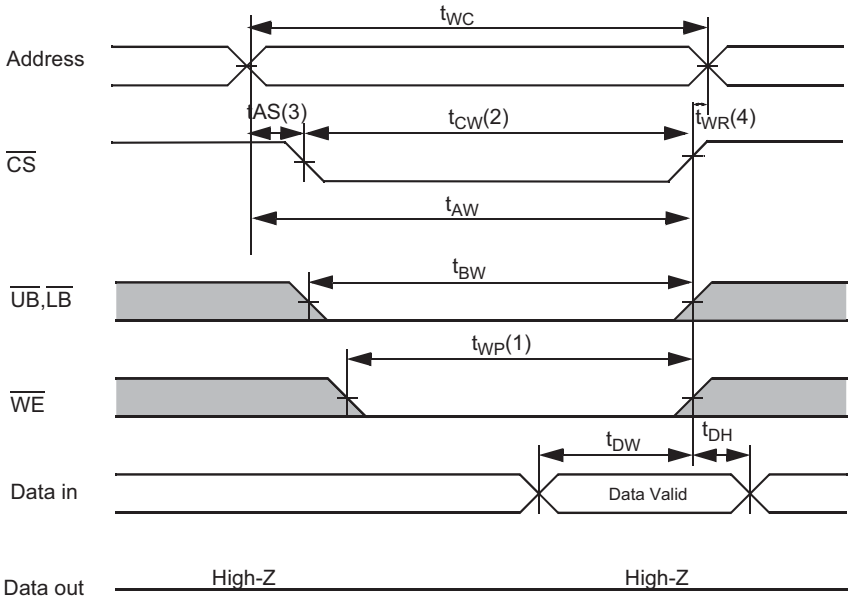
Notes(Read Cycle)

1. t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

Timing Waveform Of Write Cycle(1)($\overline{WE}$ Controlled)



Timing Waveform Of Write Cycle(2)($\overline{CS}$ Controlled)



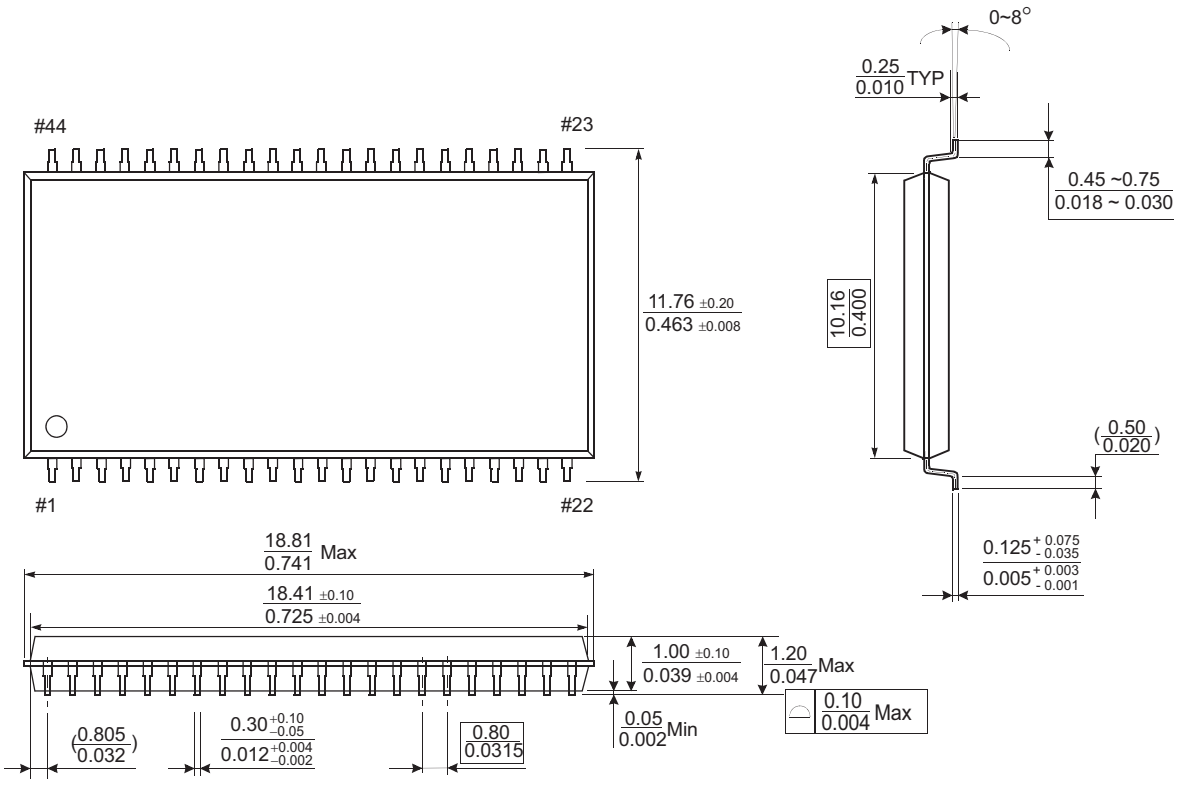
Notes(Write Cycle)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

Package Dimensions

44pin TSOP-Type2

Units:millimeters/Inches

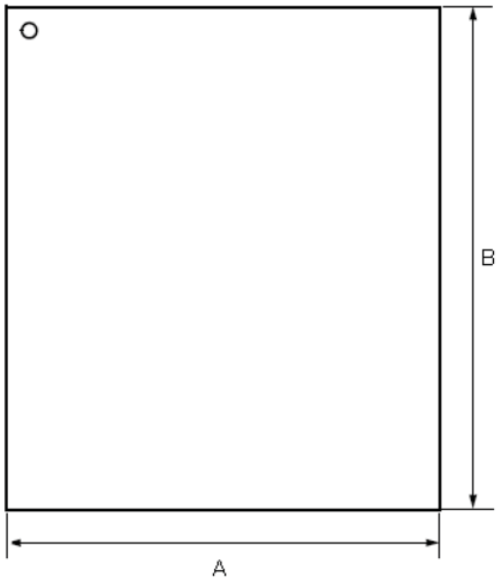


Package Dimensions

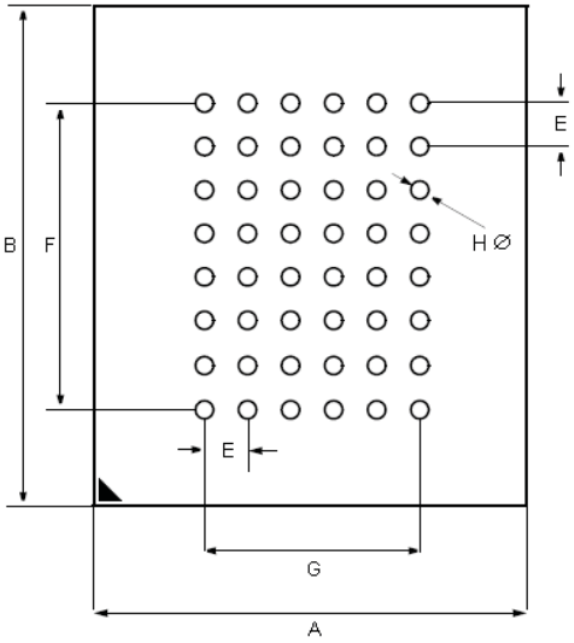
48 Balls FBGA

Units:millimeters/Inches

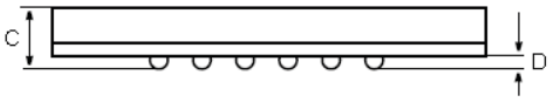
Top View



Bottom View



Side View



Symbol	Value	Units	Note
A	6±0.1	mm	
B	8±0.1	mm	
C	1.1±0.1	mm	
D	0.25±0.05	mm	
E	0.75	mm	
F	5.25	mm	
G	3.75	mm	
H	0.35±0.05	mm	

Ordering Information

Part Number	Density	Org.	V_{cc}	Access Times	Temp.	Package
EMI504NL16VM-55IT	4Mbit	256K*16bit	2.7V~ 3.6V	55ns	-40~85°C	44TSOP2
EMI504NL16LM-55IT	4Mbit	256K*16bit	2.7V~ 3.6V	55ns	-40~85°C	48FBGA

Code Informations

X	X	X	X	X	X	X	X	X	X	X	X	-	X	X	X	X	X	X
1	2	3	4	5	6	7	8	9	10	11	12		13	14	15	16	17	18

Digit-No.	Remark		Code
1,2,3	Energeic Microelectronics Inc.Product		EMI
4	Asynchronous SRAM		5
5,6	Density	1Mb	01
		2Mb	02
		4Mb	04
		8Mb	08
		16Mb	16
		32Mb	32
7	Vcc	1.8V	L
		3.3V	N
		5.0V	H
		1.65V~3.6V	W
8	Product type	Low Power(1 C/S)	L
		Low Power(2C/S)	B
		Fast	F
9,10	Organization	8bit	08
		16bit	16
11	Package	36 BGA	N
		48 BGA	L
		48 TSOP1	T
		44 TSOPII	V
		32 TSOP1	S
		32 sTSOP1	W
		32 TSOPII	Y
		32 SOP	P
12	Die Version	Monther Die	M
		2nd Generation	A
		3rd Generation	B
13,14	Speed	8ns	08
		10ns	10
		12ns	12
		45ns	45
		55ns	55
15	Temperature range	-40℃ to 85℃	I
		-40℃ to 105℃	A
16	Packing type	Tray	Blank
		Tape and Reel	T
17，18	Special function	TBD	TBD

深圳市英尚微电子有限公司
Web: www.sramsun.com
Tel: 0755-66658299
Email: sales@sramsun.com