8Mbit Full CMOS RAM

FEATURES

- Process Technology : Full CMOS
- Organization : 512K x 16
- Power Supply Voltage : 2.7~3.3V
- Three state output and TTL Compatible
- Package Type: 48-FBGA-6.00x8.00 mm
- Separated I/O power(VCCQ) & Core Power(VCC)
- Automatic power-down when deselected

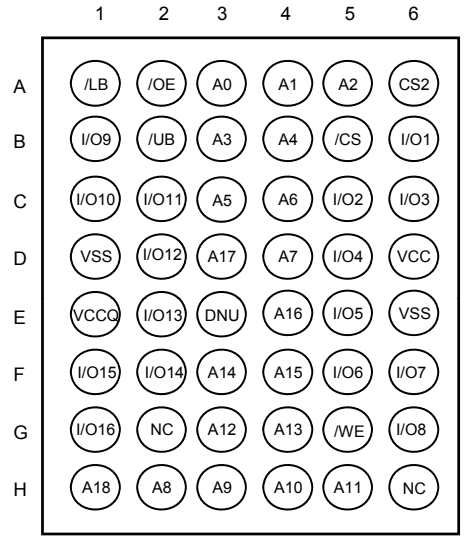
DESCRIPTION

This device is a full COMS SRAM which uses DRAM type memory cells, but thisdevice has refresh-free operation and extreme low power consumption technology.
Furthermore the inter-face is compatible to a low power Asynchronous type SRAM.

PRODUCT FAMILY

Product Family	Operating Temperature	Operating Voltage (V)			Speed	Power Dissipation					
						ICC1		ICC2		ISB1 (CMOS Standby Current)	
						f = 1MHz		f = fmax			
		Min.	Typ.	Max.		Typ.	Max.	Typ.	Max.	Typ.	Max.
EMI108NA16LM-70I	Industrial (-40~85'C)	2.7	3.0	3.3	70ns	1.5mA	3mA	15mA	25mA	30uA	70uA

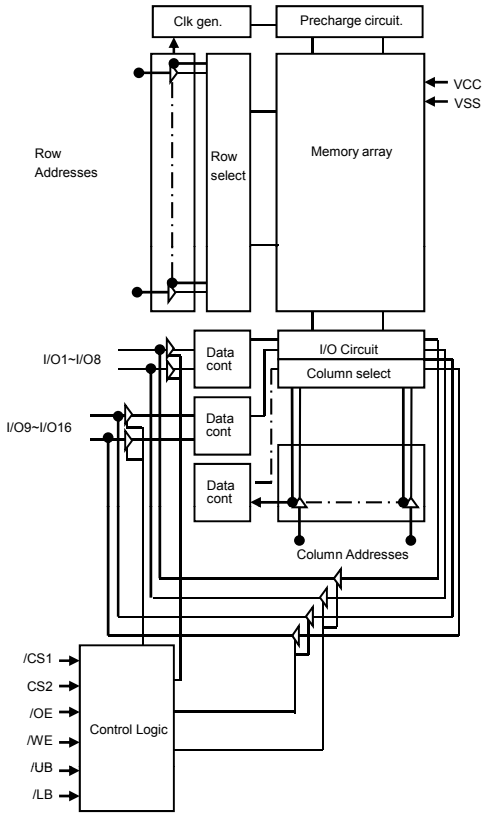
PIN DESCRIPTION



48-FBGA : Top View(Ball Down)

Name	Function	Name	Function
CS2	Chip Select Input	VCC	Core Power
/CS1	Chip Select Input	VCCQ	I/O Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
A0~A18	Address Inputs	/LB	Lower Byte(I/O 1~8)
I/O1~I/O16	Data Inputs/Outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

/CS1	CS2	/OE	/WE	/LB	/UB	I/O1-8	I/O9-16	Mode	Power
H	X[1)]	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselect/Power-down	Standby
X[1)]	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselect/Power-down	Standby
X[1)]	X[1)]	X[1)]	X[1)]	H	H	High-Z	High-Z	Deselect/Power-down	Standby
L	H	H	H	L	X[1)]	High-Z	High-Z	Output Disabled	Active
	H	H	H	X[1)]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
				H	L	High-Z	Dout	Upper Byte Read	Active
				L	L	Dout	Dout	Word Read	Active
		X[1)]	L	L	H	Din	High-Z	Lower Byte Write	Active
				H	L	High-Z	Din	Upper Byte Write	Active
				L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to Vcc+0.3V	V
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 3.6	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	'C
Operating Temperature	T_A	-40 to 85	'C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for Industrial periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	V
I/O operating voltage	V_{CCQ}	2.7	3.3	V
Ground	V_{SS}	0	0	V
Input high voltage	V_{IH}	0.8VCCQ	VCC+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	0.2VCCQ	V

Note :
1.T_A=-40 to 85'C, otherwise specified.
2. Overshoot : Vcc+1.0V in case of pulse width≤20ns.
3. Undershoot : -1.0V in case of pulse width≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz , T_A=25'C)

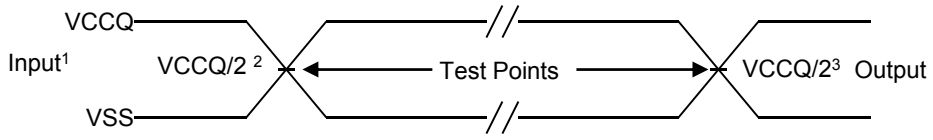
Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	CIN	VIN=0V	-	8	pF
Input/Output capacitance	CIO	VIO=0V	-	8	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	ILI	VIN=VSS to VCC	-1	-	1	uA
Output leakage current	ILO	/CS1=VIH, CS2=VIH, /OE=VIH or /WE=VIL, VIO=VSS to VCC	-1	-	1	uA
Average operating current	ICC1	Cycle time=1us, 100%duty, IIO=0mA, /CS1≤0.2V, CS2=VIH, VIN≤0.2V or VIN≥VCC-0.2V	-	1.5	3	mA
	ICC2	Cycle time=Min, IIO=0mA, 100% duty, /CS1=VIL, CS2=VIH, VIN=VIL or VIH	-	15	25	mA
Output low voltage	VOL	IOL=0.5mA			0.2VCCQ	V
Output high voltage	VOH	IOH=-0.5mA	0.8VCCQ			V
Standby Current(TTL)	ISB	/CS1=VIH, CS2=VIH, Other inputs=VIH or VIL	-	-	0.3	mA
Standby Current(CMOS)	ISB1	/CS1≥VCC-0.2V, CS2≤0.2V, Other inputs=0~VCC	-	-	70	uA

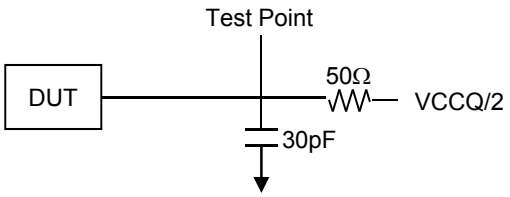
AC Input/Output Reference Waveform



NOTE:

1. AC test inputs are driven at VCCQ for a logic 1 and VSS for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at VCCQ/2.
3. Output timing ends at VCCQ/2.

AC Output Load Circuit



AC CHARACTERISTICS(VCC=2.7V~3.3V, Industrial product : T_A=-40 to 85'C)

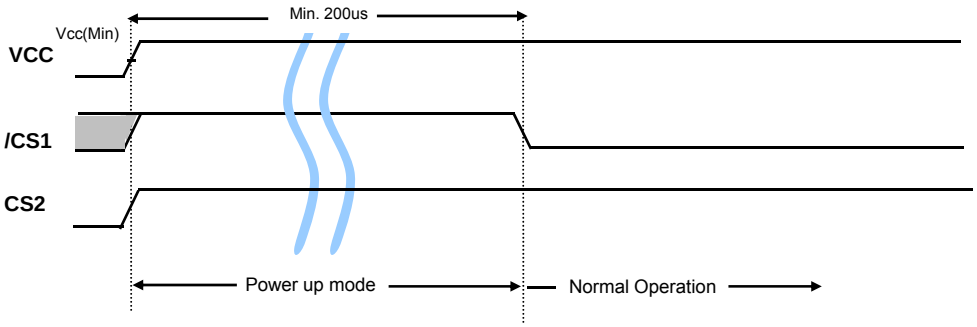
Parameter List		Symbol	70ns		Units
			Min	Max	
Read	Read Cycle Time	tRC	70	20K	ns
	Address Access Time	tAA	-	70	ns
	Chip Select to Output	tCO	-	70	ns
	Output Enable to Valid Output	tOE	-	25	ns
	/UB, /LB Access Time	tBA	-	70	ns
	Chip Select to Low-Z Output	tLZ	10	-	ns
	/UB, /LB Enable to Low-Z Output	tBLZ	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	ns
	Chip Disable to High- Z Output	tHZ	0	5	ns
	/UB, /LB Disable to High- Z Output	tBHZ	0	5	ns
	Output Disable to High- Z Output	tOHZ	0	5	ns
	Output Hold from Address Change	tOH	5	-	ns
Write	Write Cycle Time	tWC	70	20K	ns
	Chip Select to End of Write	tCW	55	-	ns
	Address Set-up Time	tAS	0	-	ns
	Address Valid to End of Write	tAW	55	-	ns
	/UB, /LB Valid to End of Write	tBW	55	-	ns
	Write Pulse Width	tWP	50	-	ns
	Write Recovery Time	tWR	0	-	ns
	Write to Output High-Z	tWHZ	0	5	ns
	Data to Write Time Overlap	tDW	20	-	ns
	Data Hold from Write Time	tDH	0	-	ns
	End Write to Output Low-Z	tOW	5	-	ns
/CS1 High Pulse Width[1)]		tCP	10	-	ns

1. /CS1 High Pulse Width is defined by /CS1 or (/UB and /LB) because /UB & /LB can make standby mode when /UB=High and /LB=High.

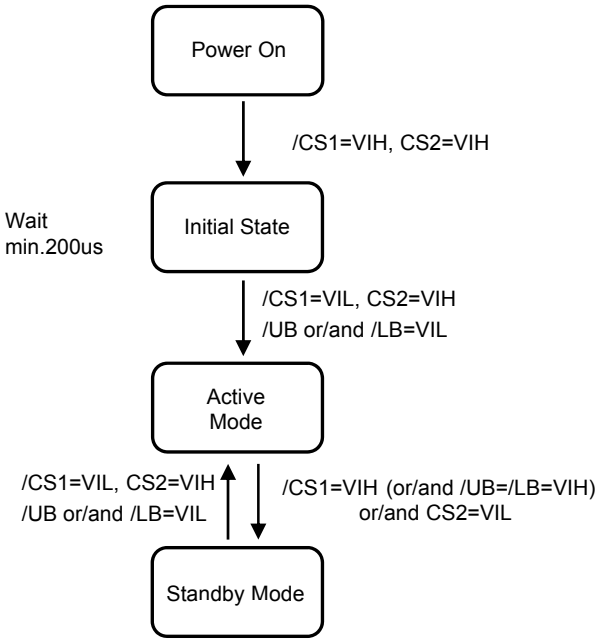
Power Up Sequence

1. Apply Power
2. Maintain stable power for a minimum of 200us with /CS1=VIH

Timing Waveform of Power Up



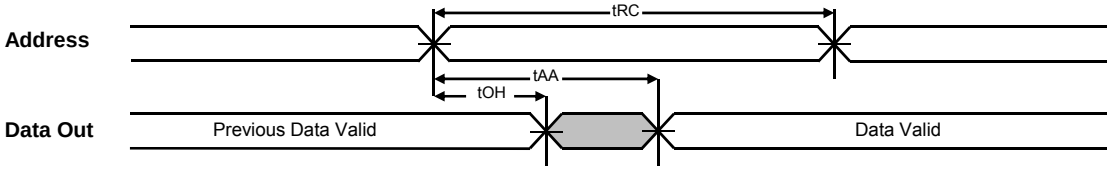
Standby Mode State machines



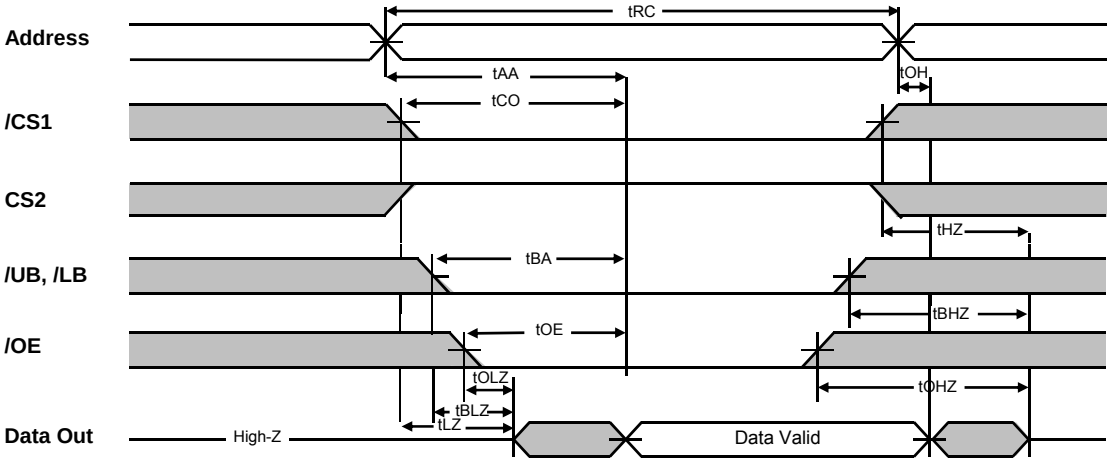
Standby Mode Characteristics

Mode	Memory Cell Data	Standby Current(uA)	Wait Time(us)
Standby	Valid	70 (ISB1)	0

READ CYCLE (1) (Address controlled,/CS1=/OE=VIL, CS2=/WE=VIH, /UB or/and /LB=VIL)

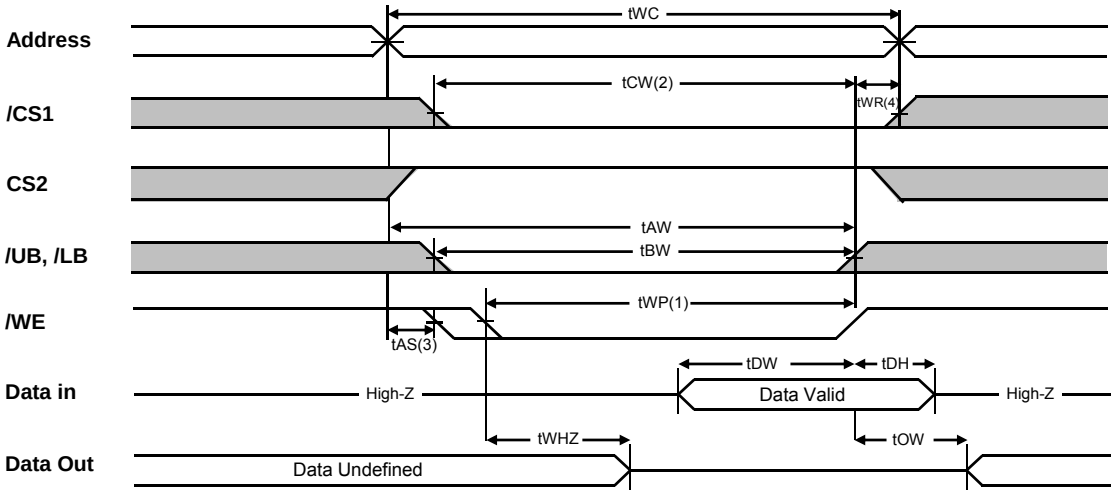


READ CYCLE (2) (CS2=/WE=VIH)

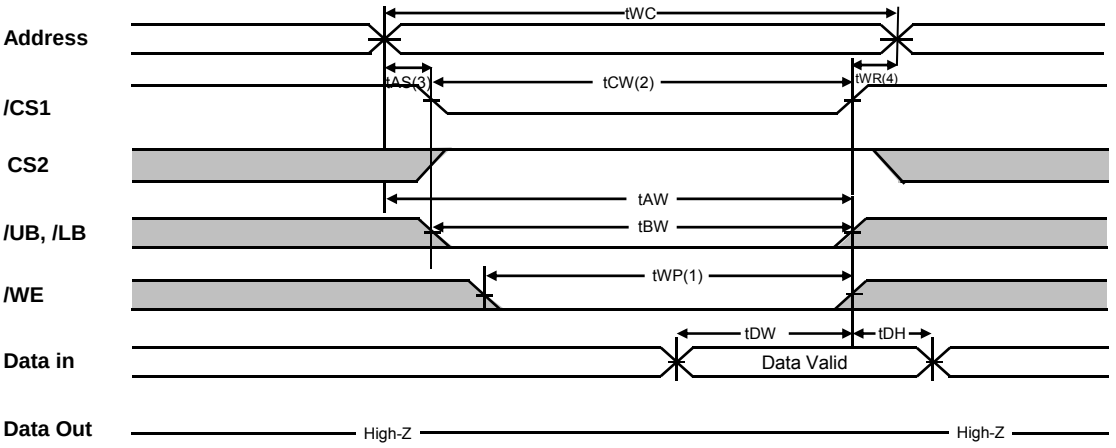


1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 20us.

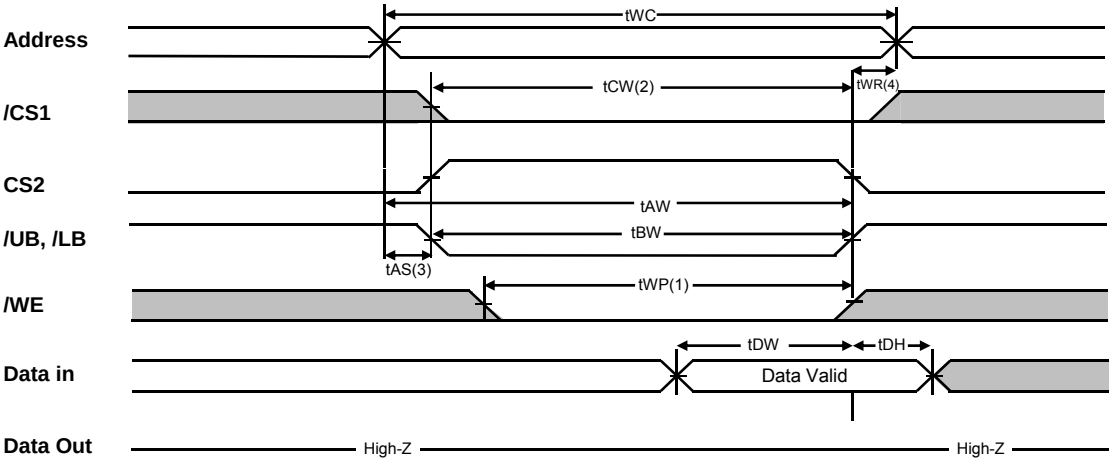
WRITE CYCLE (1) (/WE controlled)



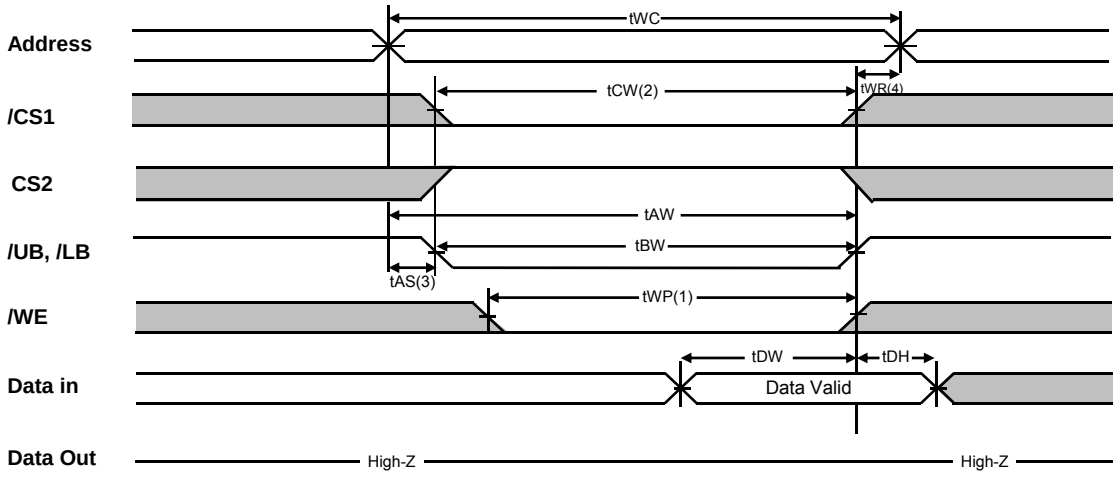
WRITE CYCLE (2) (/CS1 controlled)



WRITE CYCLE (3) (CS2 controlled)



WRITE CYCLE (4) (/UB, /LB controlled)



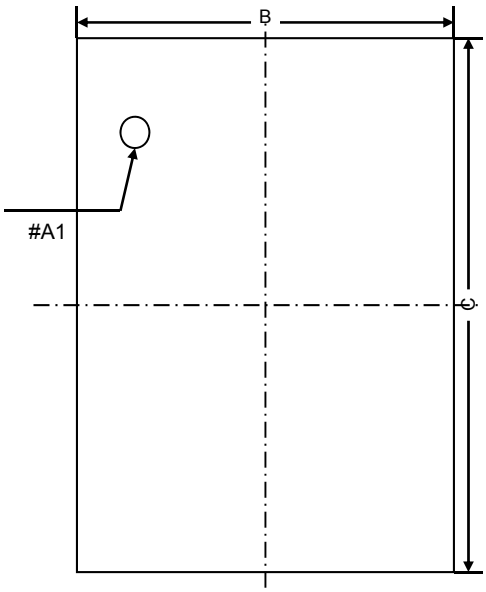
1. A write occurs during the overlap (tWP) of low /CS1 and /WE. A write begins when /CS1 goes low and /WE goes low with asserting /UB or /LB for single byte operation or simultaneously asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CS1 goes high and /WE goes high. The tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the /CS1 going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS1 or /WE going high.
5. Do not access device with cycle timing shorter than tRC(tWC) for continuous periods > 20us.

PACKAGE DIMENSION

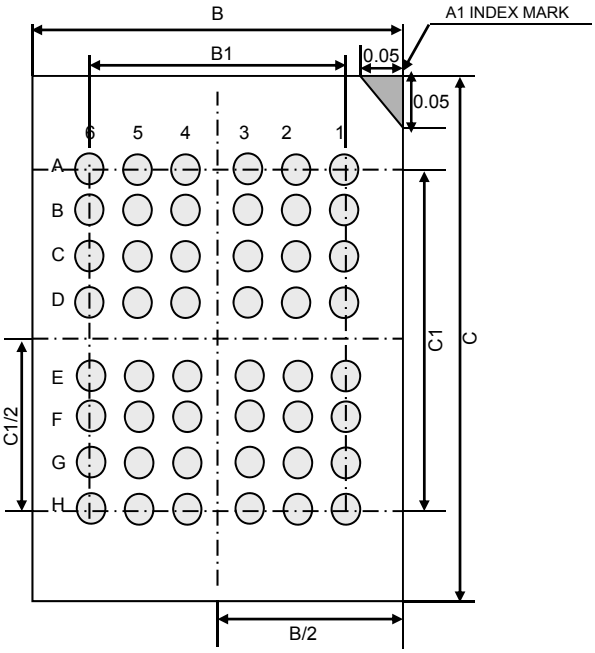
Unit : millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)

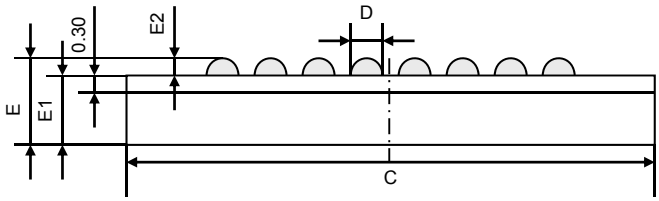
Top View



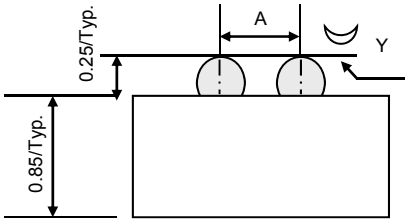
Bottom View



Side View



Detail A



-	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.10	1.20
E1	-	0.85	-
E2	0.20	0.25	0.30
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)